MT6572 HSPA Smartphone Application Processor Technical

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Document Revision History

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

MT6572 is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable 3G smart phone applications, with integrated Bluetooth, WiLAN and GPS modules. The chip integrates a Dual-core ARM® Cortex-A7 MPCore™ operating up to 1.2GHz, an ARM® Cortex-R4 MCU and a powerful multi-standard video accelerator. MT6572 supports various interfaces, including parallel/serial NAND flash memory and 32-bit LPDDR2 for optimal performance, and supports booting from SLC NAND or eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards.

The application processor, a Dual-core ARM® Cortex-A7 MPCore™ which includes a NEON multimedia processing engine, offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Audio supported includes FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting WCDMA Category 14 (21 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates or TD-SCDMA Category 14 (2.8 Mbps) HSDPA downlink, Category 6 (2.2 Mbps) HSUPA , as well as Class 12 GPRS and EDGE.

MT6572 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6572 provides the best and most convenient connectivity solution among the industry. MT6572 implements advanced and sophisticated radio coexistence algorithms and hardware mechanisms. It also supports single antenna sharing among 2.4 GHz antenna for Bluetooth, WLAN and 1.575 GHz for GPS.

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1.1 Platform Features

- **General**
  - Smartphone,3 MCU subsystems architecture
  - SLC NAND flash and eMMC bootloader
  - Supports LPDDR-1/LPDDR-2/LPDDR-3/PD-DDR3

- **AP MCU subsystem**
  - Dual-core ARM® Cortex-A7 MPCore™ operating at 1.2GHz
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 256KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 1.05V to 1.26V

- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with maximum 480MHz operation frequency
  - 32KB I-cache, 16KB D-cache
  - 256KB TCM (tightly-coupled memory)
  - DSP for running modem/voice tasks, with maximum 245.76MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Supports dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, …)
  - UART for modem logging/debugging purpose

- **External memory interface**
  - Supports LPDDR1/2/3, PC-DDR3 up to 2GB
  - 32-bit data bus width
  - Memory clock up to 333MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 high-speed OTG supporting 8 Tx and 8 Rx endpoints
  - USB2.0 full-speed host
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - 2 UART for debugging and applications
  - SPI for external device
  - 2 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Maximum 5 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional

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external hi-end audio codec
- GPIOs
- 2 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.15V
  - Processor DVFS voltage: 1.15V ~ 1.26V (Typ. 1.15V; sleep mode 1.05V)
  - Processor SRAM voltage: 1.15V ~ 1.26V (Typ. 1.15V; sleep mode 1.05V)
  - GPU voltage: 1.15V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V/1.8V/1.35V/1.5V
  - NAND: 1.8V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: TFBGA
  - 10.6mm x 10.6mm
  - Height: 1.1mm maximum
  - Ball count: 428 balls
  - Ball pitch: 0.4mm

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1.2 MODEM Features

- **3G UMTS FDD supported features (with MT6166)**
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - MAC-ehs
  - Uplink Cat.6, throughput up to 5.7Mbps
  - Downlink Cat. 14, throughput up to 21Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **3G TDD supported features**
  - TD-SCDMA/HSDPA/HSUPA baseband
  - Supports TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data, and packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength (shared by 2G & 3G modem)
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced sidetone oscillation reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (single antenna interference cancellation) technology
  - Supports VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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1.3 Connectivity Features

- **Supports integrated WIFI/BlueTooth/GPS**
  - Supports single antenna for Bluetooth and WLAN, GPS
  - Self calibration
  - Supports TCXO & TSX
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (for example, transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (Hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) Supports HotSpot 2.0 Passpoint
  - Per packet TX power control

- **BlueTooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality
  - Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Supports GPS/QZSS/SBAS (WAAS/MSAS/EGNOS/GAGAN)
  - Best-in-class sensitivity performance
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 8 in-band tones
  - Low-power operational modes
  - 5Hz update rate

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1.4 Multimedia Features

- **Display**
  - Supports landscape or portrait panel resolution up to qHD (960x540)
  - Supports 8/9/16/18-bit host interface (MIPI DBI)
  - Supports 8/9/16/18/24/32-bit serial interfaces
  - Supports landscape or portrait panel resolution up to qHD (960x540)
  - Supports 8/9/16/18-bit host interface (MIPI DBI)
  - Supports 8/9/16/18/24/32-bit serial interfaces
  - Supports 16/18/24-bit RGB interfaces (MIPI DPI)
  - MIPI DSI interface (3 data lanes)
  - Embedded LCD gamma correction
  - Supports true colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Supports spatial and temporal dithering
  - Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Supports color enhancement
  - Supports adaptive contrast enhancement
  - Supports image/video/graphic sharpness enhancement
  - Supports dynamic backlight scaling

- **Graphics**
  - OpenGL ES 1.1/2.0 3D graphic accelerator
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Supports 5 MP Capture up to 15fps
  - Supports MIPI CSI-2 high-speed camera serial interface with 2 data lane (for main) + 2 data lane (for sub)
  - Supports face detection and visual tracking
  - Supports zero shutter delay image capture
  - Supports capturing image when recording video
  - Supports JPEG decoder for baseline decoding up to 29.4M pixel/sec; supports progressive format decoding
  - Supports JPEG encoder for baseline encoding up to 17.5M pixel/sec

- **Video**
  - H.264 decoder: Baseline 720p @ 30fps
  - H.264 decoder: Main/high profile 720p@30fps
  - MPEG-4 SP/ASP decoder: 720p @ 30fps
  - DIVX3/DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 720p @ 30fps
  - VP8 decoder: 720p @ 30fps
  - VC-1 decoder: 720p @ 30fps
  - MPEG-4 encoder: Simple profile 720p @ 30fps
  - H.263 encoder: 720p @ 30fps
  - H.264 encoder: Baseline profile VGA @ 24fps

- **Audio**
  - Sampling rates supported: 8kHz to 48kHz

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- Sample formats supported: 8-bit/16-bit, Mono/Stereo
- Interfaces supported: I2S, proprietary audio interface for MT6323
- Customizable multiband loudspeaker and headphone compensation IIR filter
- MediaTek proprietaty audio post-processing, BesSound Series: BesAudEnh (earphone enhancer), BesLoudness (volume maximizer), BesSurround (virtual 3D surround), BesEQ (multiband equalizer), BesBass (bass booster), BesLive (virtual auditory space), BesRecord (mono/stereo record, up-to 48KHz sampling rate, with Stereo-widening)
- Android built-in post processing
- Audio encode: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decode: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC input
  - Digital MIC input

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1.5 General Description

MediaTek MT6572 is a highly integrated 3G System-on-chip (SoC) which incorporates advanced features, e.g. HSPA modem, Dual-core ARM® Cortex-A7 MPCore™ operating at 1.2 GHz, 3D graphics (OpenGL|ES 2.0), 5M camera, LPDDR2 up to 667MHz and high-definition 720p video decoder. MT6572 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

World-leading technology

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6572 is the brand-new generation smart phone SoC integrating MediaTek HSPA modem, 1.2GHz Dual-core ARM® Cortex-A7 MPCore™, 3D graphics and high-definition 720pp video decoder.

Rich in features, high-valued product

To enrich the camera features, MT6572 equips a 5M camera with advanced features, e.g. auto focus, anti-handshake, auto sensor defect pixel correction, continuous video AF, face detection, burst shot, optical zoom and panorama view.

Incredible browser experience

The 1.2GHz Dual-core ARM® Cortex-A7 MPCore™ with NEON multimedia processing engine brings PC-like browser experiences and helps accelerate OpenGL|ES 2.0 3D Adobe Flash 10 rendering performance to an unbeatable level.

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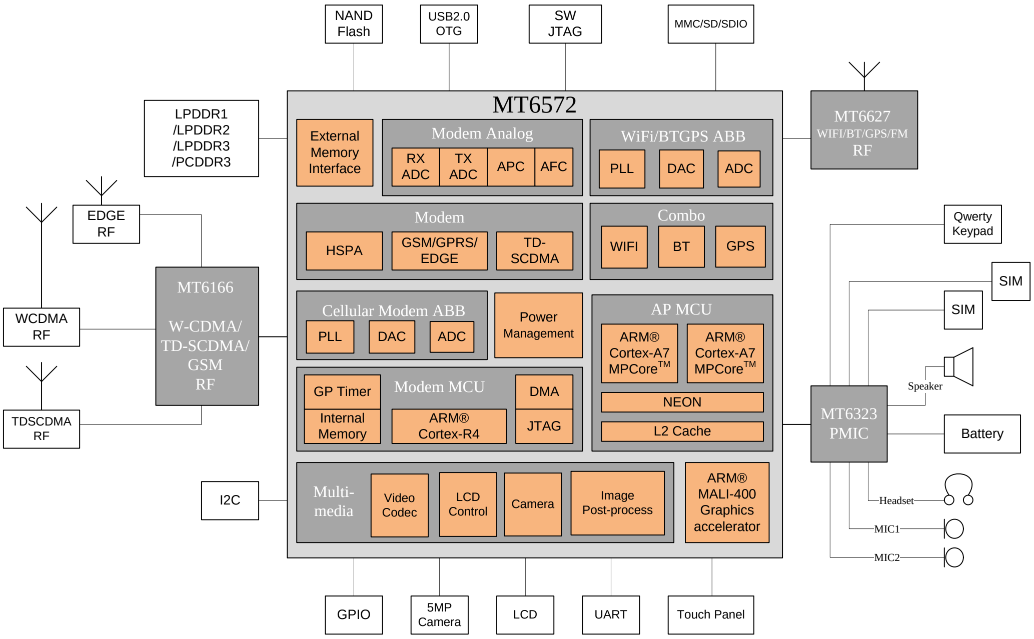

Figure 1. Block diagram of MT6572

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

428	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AVSS18_MD	UL_I_P		AVSS18_MD	AUX_IN5_YM		VM1	VM0		BPI_BUS7	BPI_BUS3		BPI_BUS6	GND_WBG		GPS_RXIP		WB_TXQP	WB_TXIN		WB_RXIN	WB_RXIP		KROW1	KCOL2	DUMMY	A
B	DL_Q_P	UL_I_N	UL_Q_N	UL_Q_P	AUX_IN3_YP	AUX_IN1	AUX_IN0	BPI_BUS13	BPI_BUS12	BPI_BUS8	BPI_BUS1	BPI_BUS0		GPS_RXQN	GPS_RXQP	GPS_RXIN		WB_TXQN	WB_TXIP	WB_RXQN	WB_RXQP	GND_WBG	SDA_1	SCL_1	KROW0	KROW2	B
C	DL_Q_N	DL_I_N	AVSS18_MD	AUX_IN4_XM	AUX_IN2_XP		BSI_DATA1			DVDD28_BPI	BPI_BUS5	BPI_BUS2		CONN_RSTB	GND_WBG	GND_WBG	GND_WBG	GND_WBG	GND_WBG	GND_WBG	GND_WBG	CONN_WB_CTRL4	CONN_WB_CTRL5	KCOL0	SCL_0	SDA_0	C
D		DL_I_P	AVDD18_MD		TXBPI	BSI_DATA2	BPI_BUS15			BPI_BUS9	BPI_BUS4	PWM_A				GND_WBG	GND_WBG	GND_WBG	GND_WBG	GND_WBG		CONN_WB_CTRL2		KCOL1	URXD1		D
E	CLK26M	AVSS18_MD			AVDD18_AP		BPI_BUS14	BPI_BUS11	BPI_BUS10			PWM_B	CONN_F2W_DAT	CONN_SDATA	CONN_SEN					CONN_WB_CTRL0		CONN_WB_CTRL3	SPI_CS		UTXD1	UTXD2	E
F	AVDD28_DAC	APC	VBIAS			REFP			BSI_DATA0		BSI_EN	CONN_F2W_CLK		CONN_XO_IN				AVDD18_WBG		CONN_WB_CTRL1			SPI_SCK	SPI_MISO	SPI_MOSI	URXD2	F
G		WATCHDOG	VSS	TESTMODE		REFN					BSI_CLK	CONN_SCLK											AVSS33_USB	AVDD33_USB	USB_DP	USB_DM	G
H		CLK32K_IN		SRCLKENA	SIM1_SCLK								DVDD18_VIO_3									CMPDN	AVDD18_USB		USB_VRT		H
J	AUD_DAT_MISO	EINTX			SIM2_SCLK			VCCK	VCCK	VCCK	VCCK			VCCK	VCCK	VCCK	VCCK		DVDD18_VIO_2			CMRST			CHD_DM	CHD_DP	J
K	AUD_DAT_MOSI	PMIC_SPI_CSN			AUD_CLK_MOSI	VCCK	VCCK	VCCK	VCCK		VCCK	VCCK		VCCK	VCCK	VCCK	VCCK			DVDD18_CAM	VSS	MC1_DAT0	MC1_CMD	DVDD3_MC1	CMRST2		K
L		PMIC_SPI_MOSI	DVDD18_VIO_1	PMIC_SPI_SCK	PMIC_SPI_MISO	VCCK	VCCK	VCCK	VCCK		VSS	VSS		VSS	VSS	VSS	VCCK				MC1_CK				CMPDN2	MC1_DAT3	L
M	SIM2_SIO	SYSRSTB	SIM1_SIO		VSS	VCCK	VCCK	VCCK	VCCK	VCCK	VSS	VSS	VSS	VSS	VSS	VSS	VCCK					MC1_DAT1			MC1_DAT2		M
N	LPD17	LPD16	LPD15	LPD13	LPD11			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS			TCP	TCN		VSS			TDN1	TDP1	N
P		LPD14			LPD9	VCCK_CPU	VCCK_CPU	VCCK_CPU	VCCK_CPU	VSS	VSS	VSS	VSS	VSS	VSS	VSS			TDN0	TDP0			TDN2	TDP2	DVSS18_MIPITX	VRT	P
R	LPD10	LPD12			LPD7	VCCK_CPU	VCCK_CPU	VCCK_CPU	VCCK_CPU	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCK				RDP1	RDN1	RDP0	RDN0	DVDD18_MIPITX	RCN	R
T	LPD8	LPD6	LPD3	LPD1	LPD5	VCCK_CPU	VCCK_CPU	VCCK_CPU	VCCK_CPU	VSS	VSS	VSS	VSS	VSS	VSS	VCCK	VCCK								DVDD18_MIPIRX	RCP	T
U		LPD4			LPD2	VCCK_CPU	VCCK_CPU		DVDD18_PLLGP	VSS	VSS	VCCK	VCCK	VCCK	VCCK	VCCK	VCCK				RDP0_A	RDN0_A			DVSS18_MIPIRX		U
V	ND15	LPD0			ND13								VSS										RDP1_A	RDN1_A	RCN_A		V
W	ND2	ND8	ND3	ND6	NCEB				VCCIO_EMI		VSS	VCCIO_EMI		VCCIO_EMI		VCCIO_EMI			VCCIO_EMI				VSS	DVDD3_LCD	RCP_A	VSS	W
Y		ND1	ND9	ND12	NWRB			EDQS2	EDQS3_B				EDQS1	EDQS0_B				EDCLK0_B	EDCLK1		VSS	CMMCLK	CMPCLK		CMDAT2	CMDAT3	Y
AA	DVDD18_MC0	ND0						EDQS2_B	EDQS3				EDQS1_B	EDQS0				EDCLK0	EDCLK1_B			LPRDB			CMDAT1		AA
AB	ND4	NREB	NWPB		VSS	ED16			ED24		VSS		EDQM0	VSS		ED0	VREF1	EA18	EA14	ECAS_B			LPA0	DVDD18_LCD	CMDAT0	LPTE	AB
AC	ND11	ND10	NCLE		ED20		ED25	VSS	ED26		VREF0		ED8		ED1			EA3			VSS	ERESET	EA12	FSOURCE	LPWRB	LRSTB	AC
AD		ND5	NALE		ED21			EDQM2			VSS	EDQM1			ED14			EA10			ERAS_B	EA11		ECKE	LPCE0B		AD
AE	ND7	ND14	NRNB	ED19	ED22	ED30	ED28	ED27	ED12	ED13	ED15	EDQM3	ED6	ED4	ED5	ED7	EA16	EA17	EA2	EA1	EA15	EA13	EA8	EA6	EA9	EA4	AE
AF	VSS	ED17	ED18		ED23	ED31		ED29	ED9		ED10	ED11	VSS		ED3	ED2		EA0	ECS1_B		EWR_B	ECS0_B		EA5	EA7	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. Ball map view for LPDDR1

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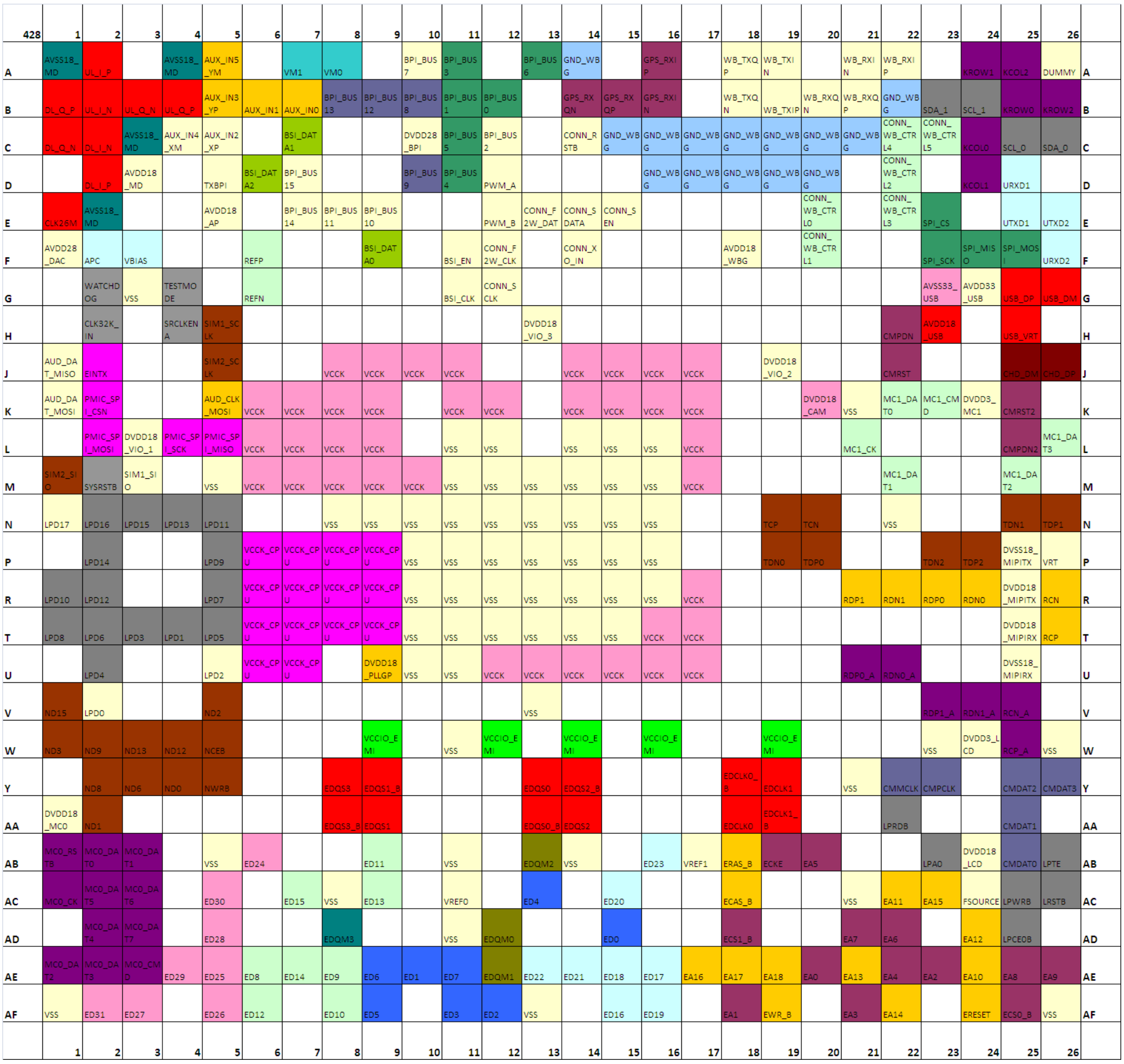

Figure 3. Ball map view for LPDDR2

2.1.2 Pin Coordinate

Table 1. Pin coordinate (use LPDDR1)

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	AVSS18_MD	K5	AUD_CLK_MOSI	U21	RDP0_A
A2	UL_I_P	K6	VCCK	U22	RDN0_A

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A4	AVSS18_MD	K7	VCCK	U25	DVSS18_MIPIRX
A5	AUX_IN5_YM	K8	VCCK	V1	ND15
A7	VM1	K9	VCCK	V2	LPD0
A8	VM0	K11	VCCK	V5	ND13
A10	BPI_BUS7	K12	VCCK	V13	VSS
A11	BPI_BUS3	K14	VCCK	V23	RDP1_A
A13	BPI_BUS6	K15	VCCK	V24	RDN1_A
A14	GND_WBG	K16	VCCK	V25	RCN_A
A16	GPS_RXIP	K17	VCCK	W1	ND2
A18	WB_TXQP	K20	DVDD18_CAM	W2	ND8
A19	WB_TXIN	K21	VSS	W3	ND3
A21	WB_RXIN	K22	MC1_DAT0	W4	ND6
A22	WB_RXIP	K23	MC1_CMD	W5	NCEB
A24	KROW1	K24	DVDD3_MC1	W9	VCCIO_EMI
A25	KCOL2	K25	CMRST2	W11	VSS
A26	DUMMY	L2	PMIC_SPI_MOSI	W12	VCCIO_EMI
B1	DL_Q_P	L3	DVDD18_VIO_1	W14	VCCIO_EMI
B2	UL_I_N	L4	PMIC_SPI_SCK	W16	VCCIO_EMI
B3	UL_Q_N	L5	PMIC_SPI_MISO	W19	VCCIO_EMI

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
B4	UL_Q_P	L6	VCCK	W23	VSS
B5	AUX_IN3_YP	L7	VCCK	W24	DVDD3_LCD
B6	AUX_IN1	L8	VCCK	W25	RCP_A
B7	AUX_IN0	L9	VCCK	W26	VSS
B8	BPI_BUS13	L11	VSS	Y2	ND1
B9	BPI_BUS12	L12	VSS	Y3	ND9
B10	BPI_BUS8	L14	VSS	Y4	ND12
B11	BPI_BUS1	L15	VSS	Y5	NWRB
B12	BPI_BUS0	L16	VSS	Y8	EDQS2
B14	GPS_RXQN	L17	VCCK	Y9	EDQS3_B
B15	GPS_RXQP	L21	MC1_CK	Y13	EDQS1
B16	GPS_RXIN	L25	CMPDN2	Y14	EDQS0_B
B18	WB_TXQN	L26	MC1_DAT3	Y18	EDCLK0_B
B19	WB_TXIP	M1	SIM2_SIO	Y19	EDCLK1
B20	WB_RXQN	M2	SYSRSTB	Y21	VSS
B21	WB_RXQP	M3	SIM1_SIO	Y22	CMMCLK
B22	GND_WBG	M5	VSS	Y23	CMPCLK
B23	SDA_1	M6	VCCK	Y25	CMDAT2
B24	SCL_1	M7	VCCK	Y26	CMDAT3

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
B25	KROW0	M8	VCCK	AA1	DVDD18_MC0
B26	KROW2	M9	VCCK	AA2	ND0
C1	DL_Q_N	M10	VCCK	AA8	EDQS2_B
C2	DL_I_N	M11	VSS	AA9	EDQS3
C3	AVSS18_MD	M12	VSS	AA13	EDQS1_B
C4	AUX_IN4_XM	M13	VSS	AA14	EDQS0
C5	AUX_IN2_XP	M14	VSS	AA18	EDCLK0
C7	BSI_DATA1	M15	VSS	AA19	EDCLK1_B
C10	DVDD28_BPI	M16	VSS	AA22	LPRDB
C11	BPI_BUS5	M17	VCCK	AA25	CMDAT1
C12	BPI_BUS2	M22	MC1_DAT1	AB1	ND4
C14	CONN_RSTB	M25	MC1_DAT2	AB2	NREB
C15	GND_WBG	N1	LPD17	AB3	NWPB
C16	GND_WBG	N2	LPD16	AB5	VSS
C17	GND_WBG	N3	LPD15	AB6	ED16
C18	GND_WBG	N4	LPD13	AB9	ED24
C19	GND_WBG	N5	LPD11	AB11	VSS
C20	GND_WBG	N8	VSS	AB13	EDQM0
C21	GND_WBG	N9	VSS	AB14	VSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C22	CONN_WB_CTRL4	N10	VSS	AB16	ED0
C23	CONN_WB_CTRL5	N11	VSS	AB17	VREF1
C24	KCOL0	N12	VSS	AB18	EA18
C25	SCL_0	N13	VSS	AB19	EA14
C26	SDA_0	N14	VSS	AB20	ECAS_B
D2	DL_I_P	N15	VSS	AB23	LPA0
D3	AVDD18_MD	N16	VSS	AB24	DVDD18_LCD
D5	TXBPI	N19	TCP	AB25	CMDAT0
D6	BSI_DATA2	N20	TCN	AB26	LPTE
D7	BPI_BUS15	N22	VSS	AC1	ND11
D10	BPI_BUS9	N25	TDN1	AC2	ND10
D11	BPI_BUS4	N26	TDP1	AC3	NCLE
D12	PWM_A	P2	LPD14	AC5	ED20
D16	GND_WBG	P5	LPD9	AC7	ED25
D17	GND_WBG	P6	VCCK_CPU	AC8	VSS
D18	GND_WBG	P7	VCCK_CPU	AC9	ED26
D19	GND_WBG	P8	VCCK_CPU	AC11	VREF0
D20	GND_WBG	P9	VCCK_CPU	AC13	ED8
D22	CONN_WB_CTRL2	P10	VSS	AC15	ED1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D24	KCOL1	P11	VSS	AC18	EA3
D25	URXD1	P12	VSS	AC21	VSS
E1	CLK26M	P13	VSS	AC22	ERESET
E2	AVSS18_MD	P14	VSS	AC23	EA12
E5	AVDD18_AP	P15	VSS	AC24	FSOURCE
E7	BPI_BUS14	P16	VSS	AC25	LPWRB
E8	BPI_BUS11	P19	TDN0	AC26	LRSTB
E9	BPI_BUS10	P20	TDP0	AD2	ND5
E12	PWM_B	P23	TDN2	AD3	NALE
E13	CONN_F2W_DAT	P24	TDP2	AD5	ED21
E14	CONN_SDATA	P25	DVSS18_MIPITX	AD8	EDQM2
E15	CONN_SEN	P26	VRT	AD11	VSS
E20	CONN_WB_CTRL0	R1	LPD10	AD12	EDQM1
E22	CONN_WB_CTRL3	R2	LPD12	AD15	ED14
E23	SPI_CS	R5	LPD7	AD18	EA10
E25	UTXD1	R6	VCCK_CPU	AD21	ERAS_B
E26	UTXD2	R7	VCCK_CPU	AD22	EA11
F1	AVDD28_DAC	R8	VCCK_CPU	AD24	ECKE
F2	APC	R9	VCCK_CPU	AD25	LPCE0B

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
F3	VBIAS	R10	VSS	AE1	ND7
F6	REFP	R11	VSS	AE2	ND14
F9	BSI_DATA0	R12	VSS	AE3	NRNB
F11	BSI_EN	R13	VSS	AE4	ED19
F12	CONN_F2W_CLK	R14	VSS	AE5	ED22
F14	CONN_XO_IN	R15	VSS	AE6	ED30
F18	AVDD18_WBG	R16	VSS	AE7	ED28
F20	CONN_WB_CTRL1	R17	VCCK	AE8	ED27
F23	SPI_SCK	R21	RDP1	AE9	ED12
F24	SPI_MISO	R22	RDN1	AE10	ED13
F25	SPI_MOSI	R23	RDP0	AE11	ED15
F26	URXD2	R24	RDN0	AE12	EDQM3
G2	WATCHDOG	R25	DVDD18_MIPITX	AE13	ED6
G3	VSS	R26	RCN	AE14	ED4
G4	TESTMODE	T1	LPD8	AE15	ED5
G6	REFN	T2	LPD6	AE16	ED7
G11	BSI_CLK	T3	LPD3	AE17	EA16
G12	CONN_SCLK	T4	LPD1	AE18	EA17
G23	AVSS33_USB	T5	LPD5	AE19	EA2
G24	AVDD33_USB	T6	VCCK_CPU	AE20	EA1
G25	USB_DP	T7	VCCK_CPU	AE21	EA15
G26	USB_DM	T8	VCCK_CPU	AE22	EA13

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
H2	CLK32K_IN	T9	VCCK_CPU	AE23	EA8
H4	SRCLKENA	T10	VSS	AE24	EA6
H5	SIM1_SCLK	T11	VSS	AE25	EA9
H13	DVDD18_VIO_3	T12	VSS	AE26	EA4
H22	CMPDN	T13	VSS	AF1	VSS
H23	AVDD18_USB	T14	VSS	AF2	ED17
H25	USB_VRT	T15	VSS	AF3	ED18
J1	AUD_DAT_MISO	T16	VCCK	AF5	ED23
J2	EINTX	T17	VCCK	AF6	ED31
J5	SIM2_SCLK	T25	DVDD18_MIPIRX	AF8	ED29
J8	VCCK	T26	RCP	AF9	ED9
J9	VCCK	U2	LPD4	AF11	ED10
J10	VCCK	U5	LPD2	AF12	ED11
J11	VCCK	U6	VCCK_CPU	AF13	VSS
J14	VCCK	U7	VCCK_CPU	AF15	ED3
J15	VCCK	U9	DVDD18_PLLGP	AF16	ED2
J16	VCCK	U10	VSS	AF18	EA0
J17	VCCK	U11	VSS	AF19	ECS1_B
J19	DVDD18_VIO_2	U12	VCCK	AF21	EWR_B
J22	CMRST	U13	VCCK	AF22	ECS0_B
J25	CHD_DM	U14	VCCK	AF24	EA5
J26	CHD_DP	U15	VCCK	AF25	EA7

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
K1	AUD_DAT_MOSI	U16	VCCK	AF26	VSS
K2	PMIC_SPI_CSN	U17	VCCK		

2.1.3 Detailed Pin Description

Table 2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. Detailed pin description (use LPDDR1)

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DIO	System reset input	DVDD18_VIO_1
WATCHDOG	DO	Watchdog reset output	DVDD18_VIO_1
TESTMODE	DIO	Test mode	DVDD18_VIO_1
RTC32K_IN	DIO	32K clock intput	DVDD18_VIO_1
SRCLKENA	DIO	26MHz co-clock enable output	DVDD18_VIO_1
PMIC			
PMIC_SPI_MOSI	DIO	PMIC SPI control interface	DVDD18_VIO_1
PMIC_SPI_MISO	DIO	PMIC SPI control interface	DVDD18_VIO_1
PMIC_SPI_CSN	DIO	PMIC SPI control interface	DVDD18_VIO_1
PMIC_SPI_SCK	DIO	PMIC SPI control interface	DVDD18_VIO_1
EINTX	DIO	PMIC SPI control interface	DVDD18_VIO_1
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD18_VIO_1
AUD_DAT_MOSI	DIO	PMIC audio input interface	DVDD18_VIO_1
ADC_DAT_MISO	DIO	PMIC audio input interface	DVDD18_VIO_1
SIM			
SIM1_SIO	DIO	SIM1 data, PMIC interface	DVDD18_VIO_1
SIM1_SCLK	DIO	SIM1 clock, PMIC interface	DVDD18_VIO_1
SIM2_SIO	DIO	SIM2 data, PMIC interface	DVDD18_VIO_1
SIM2_SCLK	DIO	SIM2 clock, PMIC interface	DVDD18_VIO_1
LCD			

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Pin name	Type	Description	Power domain
LPCE0B	DIO	Parallel display interface chip select 0 output	DVDD3_LCD/DVDD18_LCD
LPTE	DIO	Parallel display interface tearing effect	DVDD3_LCD/DVDD18_LCD
LRSTB	DIO	Parallel display interface Reset Signal	DVDD3_LCD/DVDD18_LCD
LPWRB	DIO	Parallel display interface Write Signal	DVDD3_LCD/DVDD18_LCD
LPRDB	DIO	Parallel display interface Read Signal	DVDD3_LCD/DVDD18_LCD
LPA0	DIO	Parallel display interface Address Signal	DVDD3_LCD/DVDD18_LCD
LPD17	DIO	Data pin 17 for DBI parallel LCD interface	DVDD18_VIO_1
LPD16	DIO	Data pin 16 for DBI parallel LCD interface	DVDD18_VIO_1
LPD15	DIO	Data pin 15 for DBI parallel LCD interface	DVDD18_VIO_1
LPD14	DIO	Data pin 14 for DBI parallel LCD interface	DVDD18_VIO_1
LPD13	DIO	Data pin 13 for DBI parallel LCD interface	DVDD18_VIO_1
LPD12	DIO	Data pin 12 for DBI parallel LCD interface	DVDD18_VIO_1
LPD11	DIO	Data pin 11 for DBI parallel LCD interface	DVDD18_VIO_1
LPD10	DIO	Data pin 10 for DBI parallel LCD interface	DVDD18_VIO_1
LPD9	DIO	Data pin 9 for DBI parallel LCD interface	DVDD18_VIO_1
LPD8	DIO	Data pin 8 for DBI parallel LCD interface	DVDD18_VIO_1
LPD7	DIO	Data pin 7 for DBI parallel LCD interface	DVDD18_VIO_1
LPD6	DIO	Data pin 6 for DBI parallel LCD interface	DVDD18_VIO_1
LPD5	DIO	Data pin 5 for DBI parallel LCD interface	DVDD18_VIO_1
LPD4	DIO	Data pin 4 for DBI parallel LCD interface	DVDD18_VIO_1
LPD3	DIO	Data pin 3 for DBI parallel LCD interface	DVDD18_VIO_1
LPD2	DIO	Data pin 2 for DBI parallel LCD interface	DVDD18_VIO_1
LPD1	DIO	Data pin 1 for DBI parallel LCD interface	DVDD18_VIO_1
LPD0	DIO	Data pin 0 for DBI parallel LCD interface	DVDD18_VIO_1
PWM			

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Pin name	Type	Description	Power domain
PWM_A	DIO	PWM_A	DVDD18_VIO_3
PWM_B	DIO	PWM_B	DVDD18_VIO_3
UART1			
UTXD1	DIO	UART1 TX	DVDD18_VIO_2
URXD1	DIO	UART1 RX	DVDD18_VIO_2
UART2			
UTXD2	DIO	UART2 TX	DVDD18_VIO_2
URXD2	DIO	UART2 RX	DVDD18_VIO_2
SPI			
SPI_CS	DIO	SPI chip select	DVDD18_VIO_2
SPI_MISO	DIO	SPI data in	DVDD18_VIO_2
SPI_MOSI	DIO	SPI data out	DVDD18_VIO_2
SPI_SCK	DIO	SPI clock	DVDD18_VIO_2
BPI			
BPI_BUS0	DIO	BPI BUS0	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS1	DIO	BPI BUS1	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS2	DIO	BPI BUS2	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS3	DIO	BPI BUS3	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS4	DIO	BPI BUS4	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS5	DIO	BPI BUS5	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS6	DIO	BPI BUS6	DVDD28_BPI/DVDD18_VIO_3
BPI_BUS7	DIO	BPI BUS7	DVDD18_VIO_3
BPI_BUS8	DIO	BPI BUS8	DVDD18_VIO_3
BPI_BUS9	DIO	BPI BUS9	DVDD18_VIO_3
BPI_BUS10	DIO	BPI BUS10	DVDD18_VIO_3
BPI_BUS11	DIO	BPI BUS11	DVDD18_VIO_3
BPI_BUS12	DIO	BPI BUS12	DVDD18_VIO_3
BPI_BUS13	DIO	BPI BUS13	DVDD18_VIO_3
BPI_BUS14	DIO	BPI BUS14	DVDD18_VIO_3
BPI_BUS15	DIO	BPI BUS15	DVDD18_VIO_3
VM			
VM1	DIO	PA mode selection	DVDD18_VIO_3
VM0	DIO	PA mode selection	DVDD18_VIO_3
BSI			
BSI_EN	DIO	BSI CS	DVDD18_VIO_3
BSI_CLK	DIO	BSI CLK	DVDD18_VIO_3
BSI_DATA0	DIO	BSI DATA0	DVDD18_VIO_3
BSI_DATA1	DIO	BSI DATA1	DVDD18_VIO_3
BSI_DATA2	DIO	BSI DATA2	DVDD18_VIO_3
TXBPI	DIO	RF MT6166 TXBPI	DVDD18_VIO_3
MSDC1			
MC1_CLK	DIO	MSDC1 clock output	DVDD3_MC1/DVDD18_CAM
MC1_CMD	DIO	MSDC1 command pin	DVDD3_MC1/DVDD18_CAM
MC1_DAT0	DIO	MSDC1 data0 pin	DVDD3_MC1/DVDD18_CAM

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Pin name	Type	Description	Power domain
MC1_DAT1	DIO	MSDC1 data1 pin	DVDD3_MC1/DVDD18_CAM
MC1_DAT2	DIO	MSDC1 data2 pin	DVDD3_MC1/DVDD18_CAM
MC1_DAT3	DIO	MSDC1 data3 pin	DVDD3_MC1/DVDD18_CAM
MSDC0			
ND11/MC0_CLK	DIO	Nand-Flash Data 11 / MSDC0 clock output	DVDD18_MC0
NRNB/MC0_CMD	DIO	Parallel NAND interface chip ready input/MSDC0 command pin	DVDD18_MC0
ND10/MC0_DAT0	DIO	Nand-Flash Data 10/MSDC0 data0 pin	DVDD18_MC0
ND14/MC0_DAT1	DIO	Nand-Flash Data 14/MSDC0 data1 pin	DVDD18_MC0
NALE/MC0_DAT2	DIO	Parallel NAND interface address latch enable output/MSDC0 data2 pin	DVDD18_MC0
NREB/MC0_DAT3	DIO	Parallel NAND interface read strobe output/MSDC0 data3 pin	DVDD18_MC0
NWPB/MC0_DAT4	DIO	Parallel NAND interface write protect output/MSDC0 data4 pin	DVDD18_MC0
ND5/MC0_DAT5	DIO	Nand-Flash Data 5/MSDC0 data5 pin	DVDD18_MC0
ND7/MC0_DAT6	DIO	Nand-Flash Data 7/MSDC0 data6 pin	DVDD18_MC0
NCLE/MC0_DAT7	DIO	Parallel NAND interface command latch enable output7/MSDC0 data7 pin	DVDD18_MC0
ND4/MC0_RSTB	DIO	Nand-Flash Data 4/MSDC0 reset output	DVDD18_MC0
NFI			
NCEB	DIO	Parallel NAND interface chip select output	DVDD18_VIO_1
NWRB	DIO	Parallel NAND interface write strobe output	DVDD18_MC0
NLD0	DIO	Nand-Flash Data 0	DVDD18_MC0
NLD1	DIO	Nand-Flash Data 1	DVDD18_VIO_1
NLD2	DIO	Nand-Flash Data 2	DVDD18_VIO_1
NLD3	DIO	Nand-Flash Data 3	DVDD18_VIO_1
NLD6	DIO	Nand-Flash Data 6	DVDD18_VIO_1
NLD8	DIO	Nand-Flash Data 8	DVDD18_VIO_1
NLD9	DIO	Nand-Flash Data 9	DVDD18_MC0
NLD12	DIO	Nand-Flash Data 12	DVDD18_MC0
NLD13	DIO	Nand-Flash Data 13	DVDD18_VIO_1
NLD15	DIO	Nand-Flash Data 15	DVDD18_VIO_1
EFUSE			
FSOURCE	DIO	E-FUSE blowing power control	FSOURCE
EMI			

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Pin name	Type	Description	Power domain
ERESET	DIO	DDR3 reset output #	VCCIO_EMI
EDCLK0	DIO	DRAM clock 0 output	VCCIO_EMI
EDCLK0_B	DIO	DRAM clock 0 output #	VCCIO_EMI
EDCLK1	DIO	DRAM clock 1 output	VCCIO_EMI
EDCLK1_B	DIO	DRAM clock 1 output #	VCCIO_EMI
ECKE	DIO	DRAM command output CKE	VCCIO_EMI
ECS0_B	DIO	DRAM chip select 0 #	VCCIO_EMI
ECS1_B	DIO	DRAM chip select 1 #	VCCIO_EMI
ECAS_B	DIO	DRAM command output CAS#	VCCIO_EMI
ERAS_B	DIO	DRAM command output RAS#	VCCIO_EMI
ERW_B	DIO	DRAM command output WR#	VCCIO_EMI
EA0	DIO	DRAM address output 0	VCCIO_EMI
EA1	DIO	DRAM address output 1	VCCIO_EMI
EA2	DIO	DRAM address output 2	VCCIO_EMI
EA3	DIO	DRAM address output 3	VCCIO_EMI
EA4	DIO	DRAM address output 4	VCCIO_EMI
EA5	DIO	DRAM address output 5	VCCIO_EMI
EA6	DIO	DRAM address output 6	VCCIO_EMI
EA7	DIO	DRAM address output 7	VCCIO_EMI
EA8	DIO	DRAM address output 8	VCCIO_EMI
EA9	DIO	DRAM address output 9	VCCIO_EMI
EA10	DIO	DRAM address output 10	VCCIO_EMI
EA11	DIO	DRAM address output 11	VCCIO_EMI
EA12	DIO	DRAM address output 12	VCCIO_EMI
EA13	DIO	DRAM address output 13	VCCIO_EMI

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Pin name	Type	Description	Power domain
EA14	DIO	DRAM address output 14	VCCIO_EMI
EA15	DIO	DRAM address output 15	VCCIO_EMI
EA16	DIO	DRAM address output 16	VCCIO_EMI
EA17	DIO	DRAM address output 17	VCCIO_EMI
EDQM0	DIO	DRAM DQM 0	VCCIO_EMI
EDQM1	DIO	DRAM DQM 1	VCCIO_EMI
EDQM2	DIO	DRAM DQM 2	VCCIO_EMI
EDQM3	DIO	DRAM DQM 3	VCCIO_EMI
EDQS0	DIO	DRAM DQS 0	VCCIO_EMI
EDQS0_B	DIO	DRAM DQS 0 #	VCCIO_EMI
EDQS1	DIO	DRAM DQS 1	VCCIO_EMI
EDQS1_B	DIO	DRAM DQS 1 #	VCCIO_EMI
EDQS2	DIO	DRAM DQS 2	VCCIO_EMI
EDQS2_B	DIO	DRAM DQS 2 #	VCCIO_EMI
EDQS3	DIO	DRAM DQS 3	VCCIO_EMI
EDQS3_B	DIO	DRAM DQS 3 #	VCCIO_EMI
ED0	DIO	DRAM data pin 0	VCCIO_EMI
ED1	DIO	DRAM data pin 1	VCCIO_EMI
ED2	DIO	DRAM data pin 2	VCCIO_EMI
ED3	DIO	DRAM data pin 3	VCCIO_EMI
ED4	DIO	DRAM data pin 4	VCCIO_EMI
ED5	DIO	DRAM data pin 5	VCCIO_EMI
ED6	DIO	DRAM data pin 6	VCCIO_EMI
ED7	DIO	DRAM data pin 7	VCCIO_EMI
ED8	DIO	DRAM data pin 8	VCCIO_EMI
ED9	DIO	DRAM data pin 9	VCCIO_EMI
ED10	DIO	DRAM data pin 10	VCCIO_EMI
ED11	DIO	DRAM data pin 11	VCCIO_EMI
ED12	DIO	DRAM data pin 12	VCCIO_EMI
ED13	DIO	DRAM data pin 13	VCCIO_EMI
ED14	DIO	DRAM data pin 14	VCCIO_EMI
ED15	DIO	DRAM data pin 15	VCCIO_EMI
ED16	DIO	DRAM data pin 16	VCCIO_EMI
ED17	DIO	DRAM data pin 17	VCCIO_EMI
ED18	DIO	DRAM data pin 18	VCCIO_EMI
ED19	DIO	DRAM data pin 19	VCCIO_EMI
ED20	DIO	DRAM data pin 20	VCCIO_EMI
ED21	DIO	DRAM data pin 21	VCCIO_EMI
ED22	DIO	DRAM data pin 22	VCCIO_EMI
ED23	DIO	DRAM data pin 23	VCCIO_EMI
ED24	DIO	DRAM data pin 24	VCCIO_EMI
ED25	DIO	DRAM data pin 25	VCCIO_EMI

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Pin name	Type	Description	Power domain
ED26	DIO	DRAM data pin 26	VCCIO_EMI
ED27	DIO	DRAM data pin 27	VCCIO_EMI
ED28	DIO	DRAM data pin 28	VCCIO_EMI
ED29	DIO	DRAM data pin 29	VCCIO_EMI
ED30	DIO	DRAM data pin 30	VCCIO_EMI
ED31	DIO	DRAM data pin 31	VCCIO_EMI
VREF0 VREF1	DIO	VREF for DRAM IO	VCCIO_EMI
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_LCD
CMMCLK	DIO	Master clock to sensor	DVDD18_LCD
CMDAT0	DIO	Pixel data[0] from sensor	DVDD18_LCD
CMDAT1	DIO	Pixel data[1] from sensor	DVDD18_LCD
CMDAT2	DIO	Pixel data[2] from sensor	DVDD18_LCD
CMDAT3	DIO	Pixel data[3] from sensor	DVDD18_LCD
CMRST	DIO	Reset control to 1st sensor	DVDD18_CAM
CMPDN	DIO	Power down to 1st sensor	DVDD18_CAM
CMRST2	DIO	Reset control to 2nd sensor	DVDD18_CAM
CMPDN2	DIO	Power down to 2nd sensor	DVDD18_CAM
I2C0			
SCL_0	DIO	I2C0 clock	DVDD18_VIO_2
SDA_0	DIO	I2C0 data	DVDD18_VIO_2
I2C1			
SCL_1	DIO	I2C1 clock	DVDD18_VIO_2
SDA_1	DIO	I2C1 data	DVDD18_VIO_2
CONN			
CONN_WB_CTRL5	DIO	WB control for CONN_RF	DVDD18_VIO_2
CONN_WB_CTRL4	DIO	WB control for CONN_RF	DVDD18_VIO_2
CONN_WB_CTRL3	DIO	WB control for CONN_RF	DVDD18_VIO_2
CONN_WB_CTRL2	DIO	WB control for CONN_RF	DVDD18_VIO_2
CONN_WB_CTRL1	DIO	WB control for CONN_RF	DVDD18_VIO_2
CONN_WB_CTRL0	DIO	WB control for CONN_RF	DVDD18_VIO_2
CONN_RSTB	DIO	Reset for CONN_RF	DVDD18_VIO_3
CONN_SEN	DIO	SPI for CONN_RF	DVDD18_VIO_3
CONN_SCLK	DIO	SPI for CONN_RF	DVDD18_VIO_3
CONN_SDATA	DIO	SPI for CONN_RF	DVDD18_VIO_3
CONN_F2W_CLK	DIO	AUD_IN from CONN_RF	DVDD18_VIO_3
CONN_F2W_DAT	DIO	AUD_IN from CONN_RF	DVDD18_VIO_3
ABB			
UL_Q_N	AIO	UMTS uplink for UMTSTX_QN	AVDD18_MD
UL_Q_P	AIO	UMTS uplink for UMTSTX_QP	AVDD18_MD
UL_I_P	AIO	UMTS uplink for UMTSTX_IP	AVDD18_MD
UL_I_N	AIO	UMTS uplink for UMTSTX_IN	AVDD18_MD
VBIAS	AIO	3G PA analog control	AVDD28_DAC

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Pin name	Type	Description	Power domain
APC	AIO	Automatic power control for modem	AVDD28_DAC
CLK26M	AIO	26MHz clock input for AP & modem	AVDD18_MD
DL_Q_P	AIO	UMTS downlink for UMTSRX_QP	AVDD18_MD
DL_Q_N	AIO	UMTS downlink for UMTSRX_QN	AVDD18_MD
DL_I_N	AIO	UMTS downlink for UMTSRX_IN	AVDD18_MD
DL_I_P	AIO	UMTS downlink for UMTSRX_IP	AVDD18_MD
REFN	AIO	Negative reference port for internal circuit	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
AUX_IN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUX_IN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUX_IN2_XP	AIO	AuxADC channel for touch screen TP_X+	AVDD18_AP
AUX_IN3_YP	AIO	AuxADC channel for touch screen TP_Y+	AVDD18_AP
AUX_IN4_XM	AIO	AuxADC channel for touch screen TP_X-	AVDD18_AP
AUX_IN5_YM	AIO	AuxADC channel for touch screen TP_Y-	AVDD18_AP
MIPI			
TDN2	AIO	DSI0 lane2 N	DVDD18_MIPITX
TDP2	AIO	DSI0 lane2 P	DVDD18_MIPITX
TDN1	AIO	DSI0 lane1 N	DVDD18_MIPITX
TDP1	AIO	DSI0 lane1 P	DVDD18_MIPITX
TDN0	AIO	DSI0 lane0 N	DVDD18_MIPITX
TDP0	AIO	DSI0 lane0 P	DVDD18_MIPITX
TCN	AIO	DSI0 CK lane N	DVDD18_MIPITX
TCP	AIO	DSI0 CK lane P	DVDD18_MIPITX
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	DVDD18_MIPITX
RDN1	AIO	CSI0 lane1 N	DVDD18_MIPIRX
RDP1	AIO	CSI0 lane1 P	DVDD18_MIPIRX
RDN0	AIO	CSI0 lane0 N	DVDD18_MIPIRX
RDP0	AIO	CSI0 lane0 P	DVDD18_MIPIRX
RCN	AIO	CSI0 CK lane N	DVDD18_MIPIRX
RCP	AIO	CSI0 CK lane P	DVDD18_MIPIRX
RDN1_A	AIO	CSI1 lane1 N/Pixel data [7] from sensor	DVDD18_MIPIRX

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Pin name	Type	Description	Power domain
RDP1_A	AIO	CSI1 lane1 P/Pixel data [6] from sensor	DVDD18_MIPIRX
RDN0_A	AIO	CSI1 lane0 N/Pixel data [5] from sensor	DVDD18_MIPIRX
RDP0_A	AIO	CSI1 lane0 P/Pixel data [4] from sensor	DVDD18_MIPIRX
RCN_A	AIO	CSI1 CK lane P/HREF from sensor	DVDD18_MIPIRX
RCP_A	AIO	CSI1 CK lane P/VREF from sensor	DVDD18_MIPIRX
USB			
USB_DP	AIO	USB D+ differential data line	AVDD33_USB
USB_DM	AIO	USB D- differential data line	AVDD33_USB
CHD_DP	AIO	BC1.1 Charger DP	AVDD33_USB
CHD_DM	AIO	BC1.1 Charger DM	AVDD33_USB
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
WBG			
WB_RX_QN	AIO	RX_QN for WIFI/BT Rx	AVDD18_WBG
WB_RX_QP	AIO	RX_QP for WIFI/BT Rx	AVDD18_WBG
WB_RX_IP	AIO	RX_IN for WIFI/BT Rx	AVDD18_WBG
WB_RX_IN	AIO	RX_IP for WIFI/BT Rx	AVDD18_WBG
WB_TX_QP	AIO	TX_QP for WIFI/BT Tx	AVDD18_WBG
WB_TX_QN	AIO	TX_QN for WIFI/BT Tx	AVDD18_WBG
WB_TX_IN	AIO	TX_IN for WIFI/BT Tx	AVDD18_WBG
WB_TX_IP	AIO	TX_IP for WIFI/BT Tx	AVDD18_WBG
GPS_RXQN	AIO	RX_QN for GPS Rx	AVDD18_WBG
GPS_RXQP	AIO	RX_QP for GPS Rx	AVDD18_WBG
GPS_RXIP	AIO	RX_IN for GPS Rx	AVDD18_WBG
GPS_RXIN	AIO	RX_IP for GPS Rx	AVDD18_WBG
CONN_XO_IN	AIO	26MHz clock input for WBG	AVDD18_WBG
Analog power			
DVDD18_PLLGP	P	Analog power input 1.8V for PLL	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX	
AVDD28_DAC	P	Analog power input 2.8V for APC	
DVDD18_MIPITX	P	Analog power for MIPI DSI	
DVDD18_MIPIRX	P	Analog power for MIPI CSI0 & CSI1	
AVDD33_USB	P	Analog power 3.3V for USB	
AVDD18_USB	P	Analog power 1.8V for USB	

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Pin name	Type	Description	Power domain
AVDD18_WBG	P	Analog power 1.8V for WBTX, WBRX, GPSRX	
Digital power			
DVDD18_VIO_1	P	Digital power input	-
DVDD18_VIO_2	P	Digital power input	-
DVDD18_VIO_3	P	Digital power input	-
DVDD28_BPI	P	Digital power input for 2.8V BPI IO	-
VCCIO_EMI	P	Digital power input for EMI	-
DVDD18_MC0	P	Digital power input for MSDC0	-
DVDD33_MC1	P	Digital power input for MSDC1 transmitter	-
DVDD33_LCD	P	Digital power input for LCD control pins' transmitter	-
DVDD18_LCD	P	Digital power input for LCD control pins' receiver	-
DVDD18_CAM	P	Digital power input for CAM control pins	-
VCCK	P	Digital power input for core	-
VCCK_CPU	P	Digital power input for processor	-
Analog ground			
AVSS18_MD	G		
DVSS18_MIPITX	G		
DVSS18_MIPIRX	G		
AVSS33_USB	G		
GND_WBG	G		
Digital ground			
VSS	G		-

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 4. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
DVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.7	1.9	V
DVDD18_MIPIRX	Analog power for MIPI CSI0 & CSI1	1.7	1.9	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
DVDD18_VIO_1 DVDD18_VIO_2 DVDD18_VIO_3	Digital power input for 1.8V IO	1.62	1.98	V
DVDD28_BPI	Digital power input for BPI	1.7	3.6	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.98	V
DVDD3_MC1	Digital power input for MSDC1	1.7	3.6	V
DVDD3_LCD	Digital power input for LCD control pins’ transmitter	1.7	3.6	V
DVDD18_LCD	Digital power input for LCD control pins’ receiver	1.62	1.98	V
DVDD18_CAM	Digital power input for CAM control pins	1.62	1.98	V
VCCIO_EMI	Digital power input for EMI	1.08	1.98	V
VCCK	Digital power input for core	0.95	1.15	V
VCCK_CPU	Digital power input for processor	0.77	1.26	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended Operating Conditions

Table 5. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.71	1.8	1.89	V
DVDD18_MIPIRX	Analog power for MIPI CSI0 & CSI1	1.71	1.8	1.89	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
DVDD28_BPI	Digital power input for BPI	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD18_VIO1 DVDD18_VIO2 DVDD18_VIO3	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.8	1.98	V
DVDD3_MC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD3_LCD	Digital power input for LCD control pins	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD18_LCD	Digital power input for LCD control pins	1.62	1.8	1.98	V
DVDD18_CAM	Digital power input for CAM control pins	1.62	1.8	1.98	V
VCCIO_EMI	Digital power input for EMI (LPDDR1)	1.7	1.8	1.9	V
	Digital power input for EMI (LPDDR2/3)	1.08	1.2	1.32	
	Digital power input for EMI (LVDDR3)	1.215	1.35	1.485	
	Digital power input for EMI (DDR3)	1.35	1.5	1.65	
VCCK	Digital power input for core	0.85	1.15	1.20	V
VCCK_CPU	Digital power input for processor	0.85	1.15	1.20	V

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After bag opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
    - Mounted within 168 hours at factory conditions of 30°C/60% RH, or
    - Stored at 20% RH.
3. Devices require baking before mounting, if:
    - 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
    - 24 hours at 125°C +5°C/-0°C for high temperature device containers.

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2.3 EMI Timing Diagram

2.3.1 Introduction

The measurement point for all signals follows definition in JEDEC DRAM standard. Timing symbols in this section are matched with the JEDEC DRAM standard. This section describes the timing characteristics when LPDDR/LPDDR2/LPDDR2/PCDDR3 SDRAM are used.

2.3.2 EMI Clock

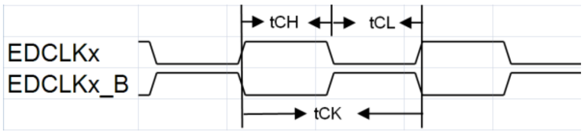

Figure 4. EMI clock EDCLKx and EDCLKx_B

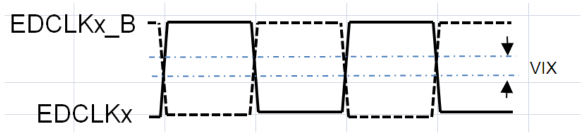

Figure 5. Differential signals of EMI clock

Table 6. EMI clock timing parameters

Symbol	Parameter	Min.	Max.	Unit
tCK	Clock cycle time	TBD	TBD	ns
tCH	Clock high-level width	0.45	0.55	tCK
tCL	Clock low-level width	0.45	0.55	tCK
VIX	Differential clock crosspoint voltage	TBD	TBD	V

2.3.3 EMI Read and Write Timing

2.3.3.1 Read and Write Timing of LPDDR1

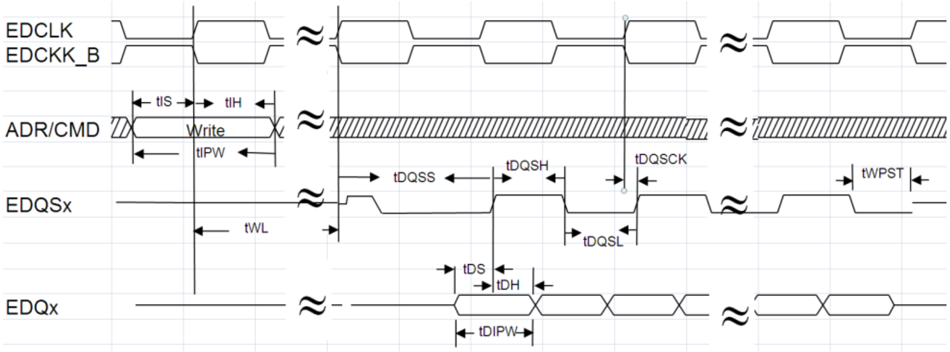

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Figure 6. EMI LPDDR1 write timing

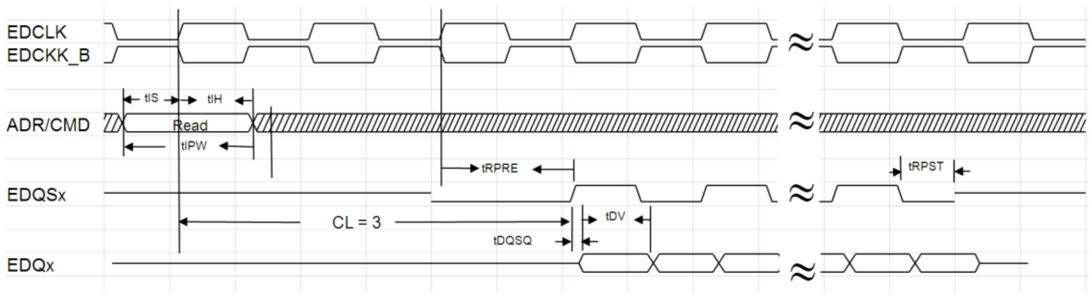

Figure 7 . EMI LPDDR1 Read timing

Table 7. EMI LPDDR1 timing parameters

Symbol	Parameter	Min.	Max.	Unit
tIS	Address and control setup input setup time	TBD	TBD	ns
tIH	Address and control input hold time	TBD	TBD	ns
tIPW	Address and control input pulse width	TBD	TBD	ns
Timing of read cycle				
tRPRE	Write preamble	TBD	TBD	tCK
tRPST	Write postamble	TBD	TBD	tCK
tDQSQ	DQS-DQ skew	TBD	TBD	ns
tDV	DQ/DQS valid window	TBD	TBD	ns
Timing of write cycle				
tDQSS	Write command to the 1st DQS latching transition	TBD	TBD	tCK
tWPST	Write postamble	TBD	TBD	tCK
tDS	DQ and DQM setup time	TBD	TBD	ns
tDH	DQ and DQM hold time	TBD	TBD	ns
tDIPW	DQ and DQM pulse width	TBD	TBD	ns
tDQSH	DQS high-level width	TBD	TBD	tCK
tDQSL	DQS low-level width	TBD	TBD	tCK
tDQSCK	DQS access time from CK/CK_B	TBD	TBD	ns

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2.3.3.2 Read and Write Timing of LPDDR2

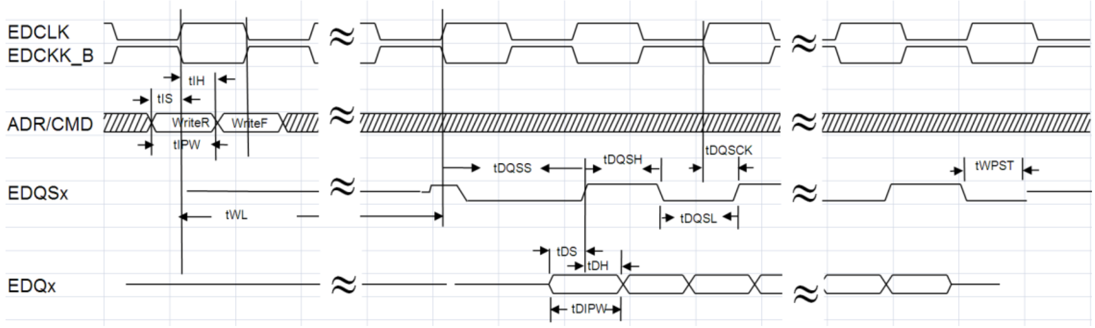

Figure 8. EMI LPDDR2 write timing

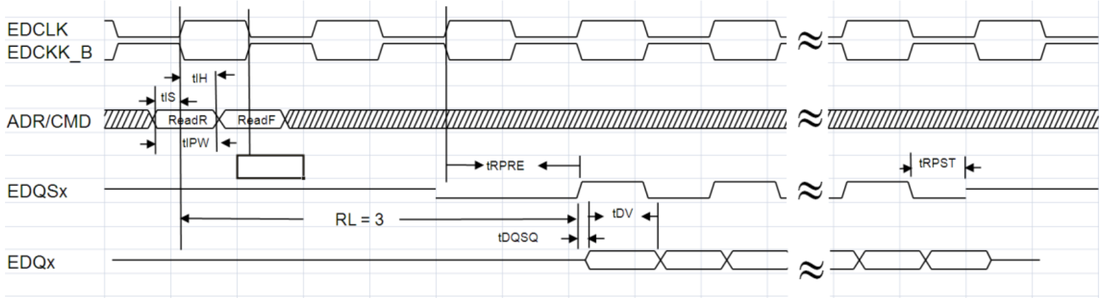

Figure 9. EMI LPDDR2 read timing

Table 8. EMI LPDDR2 timing parameters

Symbol	Parameter	Min.	Max.	Unit
tIS	Address and control setup input setup time	TBD	TBD	ns
tIH	Address and control input hold time	TBD	TBD	ns
tIPW	Address and control input pulse width	TBD	TBD	ns
Timing of read cycle				
tRPRE	Write preamble	TBD	TBD	tCK
tRPST	Write postamble	TBD	TBD	tCK
tDQSQ	DQS-DQ skew	TBD	TBD	ns
tDV	DQ/DQS valid window	TBD	TBD	ns
Timing of write cycle				
tDQSS	Write command to the 1st DQS latching transition	TBD	TBD	tCK
tWPST	Write postamble	TBD	TBD	tCK
tDS	DQ and DQM setup time	TBD	TBD	ns
tDH	DQ and DQM hold time	TBD	TBD	ns
tDIPW	DQ and DQM pulse width	TBD	TBD	ns

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Symbol	Parameter	Min.	Max.	Unit
tDQSH	DQS high-level width	TBD	TBD	tCK
tDQSL	DQS low-level width	TBD	TBD	tCK
tDQSCK	DQS access time from CK/CK_B	TBD	TBD	ns

2.3.3.3 Read and Write Timing of LPDDR3

TBD

2.3.3.4 Read and Write Timing of PCDDR3

TBD

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2.4 System Configuration

2.4.1 Mode Selection

Table 9 Mode selection

Pin name	Description
[0] PMIC_SPI_CSN [1] AUD_DAT_MOSI	00: Use pin map for LPDDR1 01: Use pin map for LPDDR2 1x: Use pin map for PCDDR3
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
BPI_BUS4	0: Boot from eMMC/NAND (default) 1: Boot from SD/SPI-NAND
[0] SIM1_SCK [1] SIM2_SCK	00: No dedicate JTAG 01: Use KP pin for S-JTAG 10: Use MC1 pins for legacy JTAG 11: Use CM pins for legacy JTAG

2.4.2 Constant Tie Pins

Table 10 Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)
FSOURCE	EFUSE burning (tied to GND)

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2.5 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

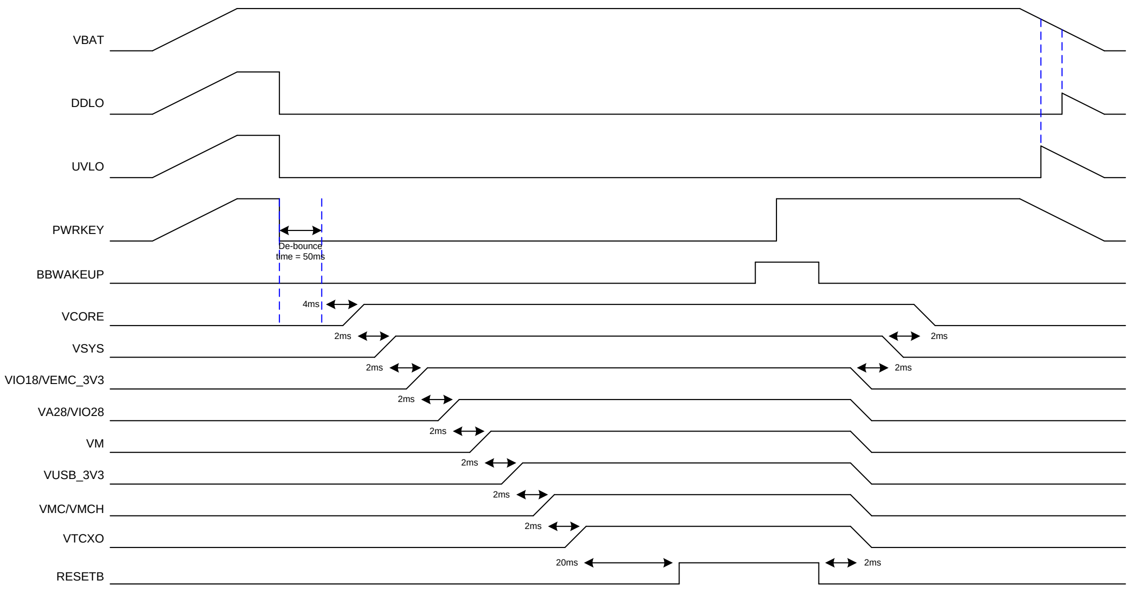

Figure 10. Power on/off sequence with XTAL

Note that the above figure only shows one power-on/off condition with XTAL. The external PMIC for application processor handles the power ON and OFF of the handset. The following three different methods switch on the handset (when VBAT ≥ 3.2V):

1. Pulling PWRKEY low (The user presses PWRKEY.)
2. Pulling BBWAKEUP high
3. Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset, which turns on regulators as long as the PWRKEY is kept low. PMIC outputs reset signal RESETB to application processor SYSRSTB input. After SYSRSTB is de-asserted, the microprocessor starts and pulls BBWAKEUP high. After that PWRKEY can be released. Pulling BBWAKEUP high will also turn on the handset. This is the case when the alarm in the RTC expires.

Besides, applying a valid external supply on CHRIN will also turn on the handset. However, if the battery is in the UV state (VBAT < 3.2V), the handset cannot be turned on in any way.

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The UVLO function in PMIC prevents system startup when the initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is bigger than 3.2V, the UVLO comparator switches and threshold are reduced to 2.9V, which allows the handset to start smoothly unless the battery decays to 2.9V and below.

Once PMIC enters the UVLO state, it draws very low quiescent current. The VRTC LDO will still be active until the DDLO disables it.

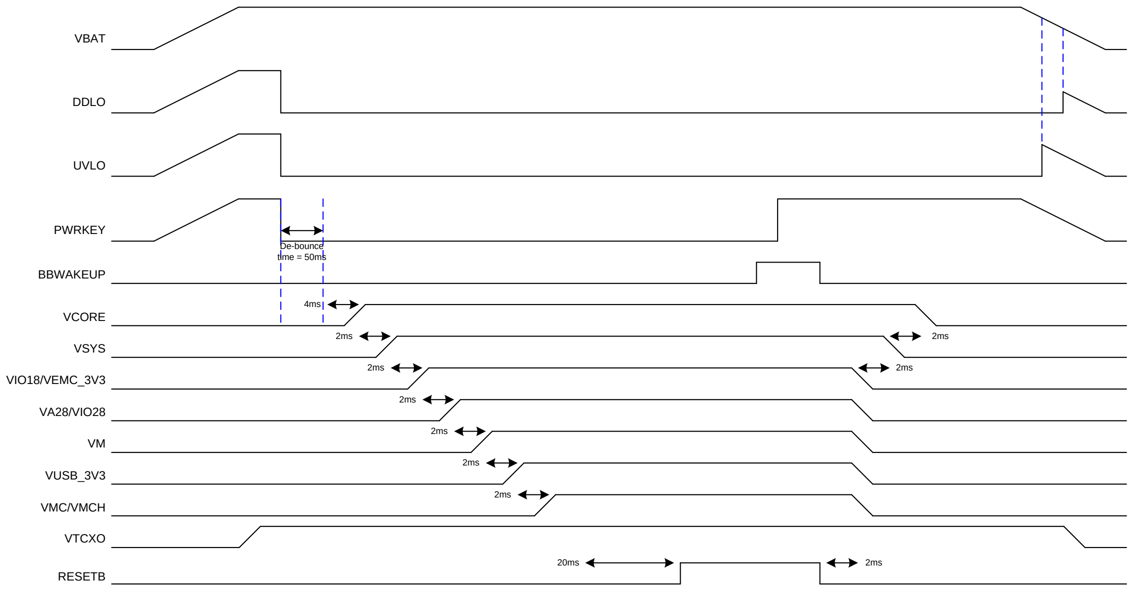

Figure 11. Power on/off sequence without XTAL

The figure above shows the power-on/off sequence without XTAL. VTCXO is always turned on when VBAT is above the DDLO threshold.

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2.6 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering.
- RF control: Two DACs for automatic power control (APC) are included. Their outputs are provided to the external RF power amplifier respectively, according to the system dual-talk configuration. One more DAC for voltage bias control (VBIAS) is included for the WCDMA system, and the output is provided to the external RF power amplifier.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: Includes two clock-squarers for shaping the dual-talk system clock and 14 PLLs providing clock signals to base-band TRx, DSP, MCUUSB, MSDC, LVDS and HDMI units.

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- APC-DAC
- VBIAS-DAC
- AUXADC
- Phase locked loop

2.6.1 BBRX

2.6.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 2 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

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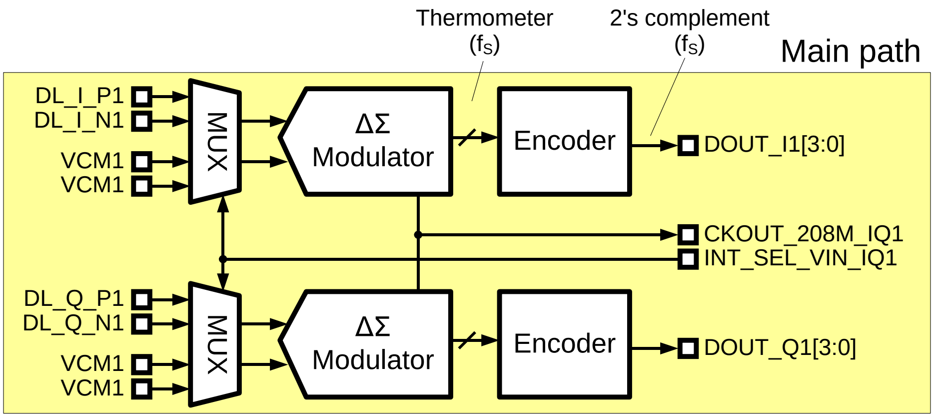

Figure 12. Block diagram of BBRX-ADC

2.6.1.2 Function Specifications

See the table below for the function specifications of the base-band downlink receiver.

Table 11. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency Clock rate (SC mode & GSM mode)		208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance SC mode & GSM mode	11.2	16	20.8	kΩ
FS	Output sampling rate		208		MSPS

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Symbol	Parameter	Min.	Typ.	Max.	Unit
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	72 84	75 87		dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down			3 1	mA uA

2.6.2 BBTX

2.6.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current, and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

The IO power, DVDD18_MD is regulated to a voltage around 1.55V to supply analog component. The required bias currents are generated by BBRX.

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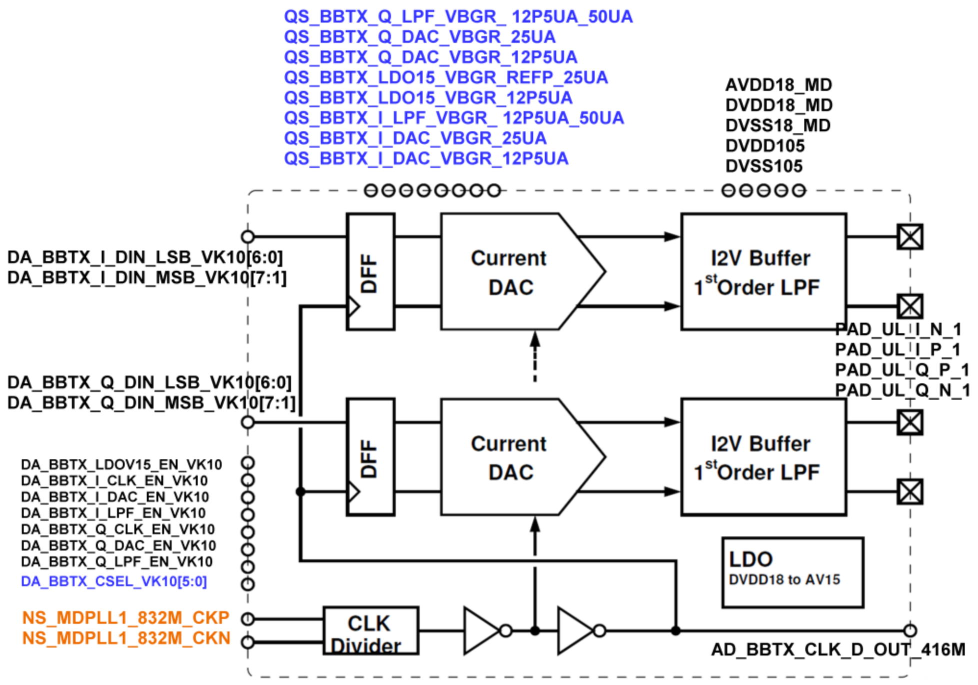

2.6.2.2 Function Specifications

Table 12. Baseband uplink transmitter specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vocm	DC output common mode voltage	0.615	0.65	0.685	V
IK	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA
Vfs	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
Fs	Sampling clock		416		MHz
Imis	1-sgma DAC unit cell mismatch			1	%
Gmis	3-sigma I/Q gain mismatch	-0.2		0.2	dB
Vos_T	3-sigma output differential DC offset over temp.			4	mV
Vos	3-sigma output differential DC offset			10	mV
F3dB	3dB corner freq.	20	25	30	MHz
SLPF	LPF selectivity @832MHz	28			dB
NOOB	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Current consumption – Power-up – Power-down		 4.1 10		 mA uA

2.6.3 APC-DAC

2.6.3.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at the APC pin.

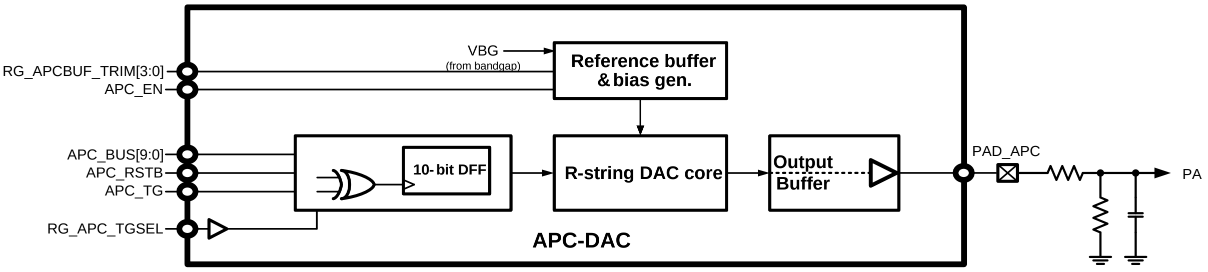

Figure 13. Block diagram of APC-DAC

2.6.3.2 Function Specifications

See the table below for the function specifications of APC-DAC.

Table 13. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		1,000	2,200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.9	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{ON}	Current consumption (power-on state)		300		uA
I_{OFF}	Current consumption (power-down state)			1	uA

2.6.4 VBIAS-DAC

2.6.4.1 Block Descriptions

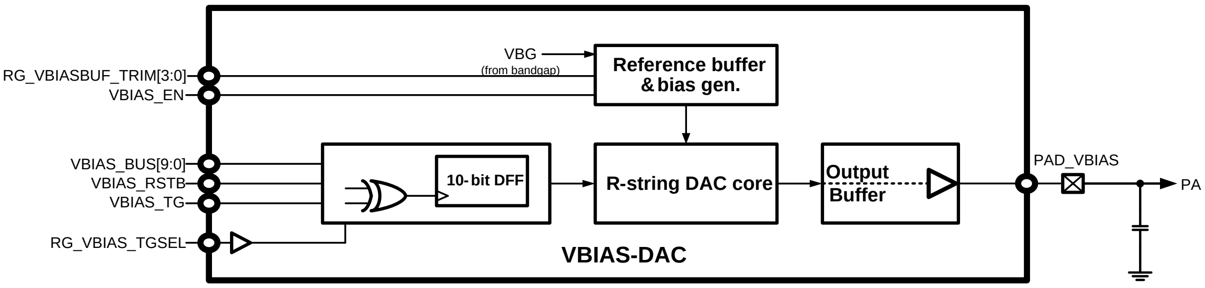

Figure 14. Block diagram of VBIAS-DAC

2.6.4.2 Function Specifications

The functional specifications of the VBIAS-DAC are listed in the following table.

Table 14. VBIAS-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10KHz sine wave with 1.0V swing)		50		dB
TS	Settling time (99% full-swing settling)			5	us
VO,max	Maximum output			AVDD – 0.2	V
CL	Output loading capacitance		1000		pF
DNL	Differential nonlinearity (code 20 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 20 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.9	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
ION	Current consumption (power-on state)		300		uA
IOFF	Current consumption (power-down state)			1	uA

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2.6.5 AUXADC

2.6.5.1 Block Descriptions

The auxiliary ADC measures ADC and is the resistive touch panel controller. The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

The touch screen controller drives the external touch panel via Pads XP, XM, YP and YM, and AUXADC as a voltage meter, obtains the X/Y-position of the touched point on the external touch screen. The touch screen interface contains 3 main blocks, which are touch screen pads control logic, ADC interface logic and interrupt generation logic. The touch screen interface supports 2 conversion modes, separate X/Y position conversion mode and auto (sequential) X/Y position conversion mode. See for brief descriptions of AUXADC input channels.

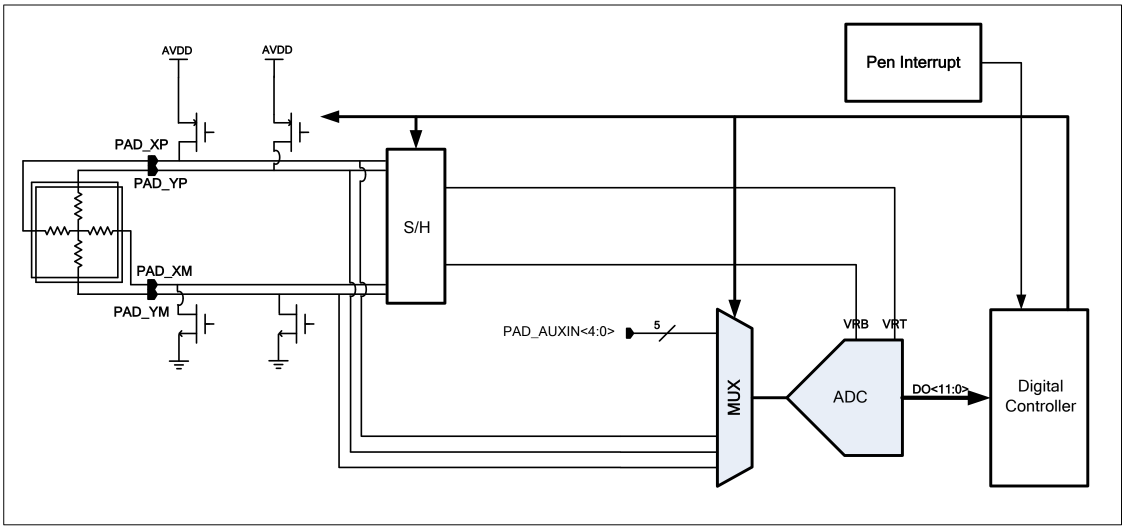

Figure 15. Block diagram of AUXADC

Table 15. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	NA

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AUXADC channel ID	Description
Channel 3	NA
Channel 4	Optional external use (AUX_IN4)
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	NA
Channel 11	NA
Channel 12	XM (touch panel)
Channel 13	XP (touch panel)
Channel 14	YP (touch panel)
Channel 15	YM (touch panel)

2.6.5.2 Function Specifications

See the table below for the function specifications of auxiliary ADC.

Table 16. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	 400			 MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+1.0/-1.0		LSB
OE	Offset error		+/- 5		mV
FSE	Full swing error		+/- 5		mV
SINAD	Signal to noise and distortion ratio (10kHz full swing input & 1.0833MHz clock rate)	62	68		dB
DVDD	Digital power supply	1.0	1.1	1.2	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog power supply	1.75	1.8	1.85	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 250 1		 uA uA
Ztp	Supports touch panel impedance	200		2K	Ω

2.6.6 Clock Squarer

2.6.6.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make MT6589 digital circuits function well. Clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.6.6.2 Function Specifications

See the table below for the function specifications of clock squarer.

Table 17. Clock squarer 1 & 2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		500		uA

2.6.7 Phase Locked Loop

2.6.7.1 Block Descriptions

There are total 10 PLLs in PLL macro, providing several clocks for CPU, BUS, modem, analog modem, GPU, Wi-Fi, BlueTooth and GPS. The usage of each PLL is listed below:

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Table 18. MT6572 PLL list

PLL	Hopping?	Reference (MHz)	Lock time (us)	Output clock frequency	Description
ARMPLL	**Hopping (0 ~ -4%)**	26	20	Range: 1000~1800Mhz Default: 1222Mhz	Cortex A7: 1001 ~ 1794zMhz Default: 1222Mhz
MAINPLL	**Hopping (0 ~ -4%)**	26	20	Range: 1000~1800Mhz Default: (1599, 1326)Mhz	EMI: 663Mhz/533MHz/399.75MHz Bus: 132.6Mhz/133.25Mhz MMSYS SMI: 265.2Mhz/266.5Mhz, e.t.c.
UNIVPLL	**fixed**	26	20	fixed: 1248Mhz	PWM: 104Mhz UART: 52Mhz MFG: 624Mhz/416MHz USB_PHY ref clock: 48Mhz, e.t.c.
WPLL	**fixed**	26	20	fixed: 491.52Mhz	FDD 3G and TDD 3G system
WHPLL	**fixed if FDD hopping if TDD (0 ~ -4%)**	26	20	FDD: fixed 500.5Mhz TDD: 520MHz ~ 491.52MHz	FDD 3G hopping clock: 500.5MHz TDD 3G hopping clock: 520Mhz ~ 491.5MHz
MCUPLL	**Hopping (0 ~ -4%)**	26	20	Default: 481Mhz	MDMCU CR4: 481Mhz FD216: 240.5Mhz MD_bus: 120.25Mhz (all down hopping 4%)
MDPLL	**fixed**	26	100 w/I Calib 20 w/o Calib	416Mhz	2G/3G modem, analog ADC, MD_UART, ..
BTPLL	**fixed**	26	150 w/I Calib 20 w/o Calib	fixed: 416Mhz	BT and ref. clock to WFPLL
WFPLL	**fixed**	26	150 w/I Calib 20 w/o Calib	fixed: 960MHz	WiFi
MIPIPLLs (macro)	**fixed/hopping**	26	20		To generate MIPI clock for DSI/CSI2/DPI (down hopping 4%)
USB20_PHYA (macro)	**fixed**	48	2O		From USB PHY/MAC

2.6.7.2 Function Specifications

See the table below for the function specifications of PLL.

Table 19. ARMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	754		1,508	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Current consumption		1.2		mA
	Power-down current consumption			1	uA

Table 20. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	500	806	884	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 21. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	624	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 22. MDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		20 w/o Calib		us

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Symbol	Parameter	Min.	Typ.	Max.	Unit
			100 w/I Calib		
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2.5		mA
	Power-down current consumption			1	uA

Table 23. WPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	245.76	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 24. WHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	250.25	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

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Table 25. MCUPLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		481		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2		mA
	Power-down current consumption			1	uA

Below table shows the function specifications of the CONN_PLL.

Table 26. BTPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	832	N/A	MHz
	Settling time		20 w/o Calib 150 w/I Calib		us
	Output clock duty cycle	47	50	53	%
PN			-80@10kHz. -87@100kHz -87@400kHz -87@1MHz -107@10MHz		dBc/(Hz)^0.5
Spur	416MHz spur		-46@2M -40@26M -40@52M -40@78M <-46@others		dBc
DVDD	Digital power supply	0.95	1.15	1.25	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

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Table 27. WFPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		32		MHz
Fout	Output clock frequency	N/A	960	N/A	MHz
	Settling time		20 w/o Calib 150 w/I Calib		us
	Output clock duty cycle	47	50	53	%
PN			-80@10kHz. -87@100kHz -87@400kHz -87@1MHz -107@10MHz		dBc/(Hz)^0.5
Spur	960MHz spur		-46@2M -40@26M -40@32M -46@64M -46@96M <-52@others		dBc
DVDD	Digital power supply	0.95	1.15	1.25	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2		mA
	Power-down current consumption			1	uA

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2.6.8 Temperature Sensor

2.6.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.6.8.2 Function Specifications

See the table below for the function specifications of temperature sensor.

Table 28. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		300		uA
	Quiescent current		3		uA

2.6.9 Connectivity ABB

The analog blocks include the following analog functions for complete connectivity analog base-band signal processing:

- WBRX, Wi-Fi and BT receiver analog based-band
- WBTX, Wi-Fi and BT transmitter analog based-band
- GPSRX, GPS receiver analog based-band

For the Wi-Fi and BT in ISM-band, there is only one ISM can be used at the same time. Use TDD (Time-Division-Duplex) to dynamically switch between Wi-Fi and BT mode.

2.6.9.1 Wi-Fi/BT RX

The Wi-Fi/BT receiver (Rx) performs connectivity baseband I/Q channels analog-to-digital conversion:

- Analog input buffer: Deliver driving capability.
- A/D converter: I/Q channels of ADCs perform I/Q digitization for further digital signal processing.

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At the same time, there is only one standard that is operating for Wi-Fi/BT (ISM-band).

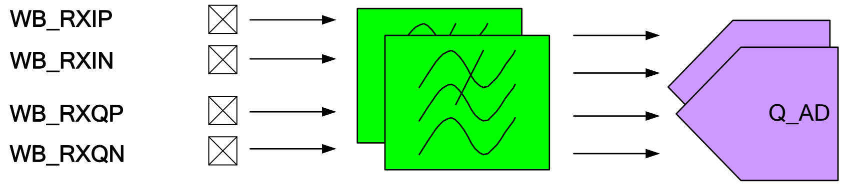

Figure 16. Wi-Fi/BT receiver analog based-band

2.6.9.2 WB RX Function Specifications

See the table below for the function specifications of the Wi-Fi/BT base-band receiver.

Table 29. Wi -Fi/BT receiver specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)		950		mV
VCM	Common mode input voltage	0.5	0.55	0.6	V
FS	Input clock frequency Clock rate (WiFi-mode) Clock rate (BT-mode)		80 32		MHz MHz
RIN	Differential input resistance WiFi-mode BT-mode	3.5 14	5 20	6.5 26	kΩ kΩ
VOS	Differential input referred offset			10	mV
DR	Dynamic range WF:Sig=20M@-10dBF BW=+-20M@fs=80M BT:Sig=1M@-10dBF BW=+1M@fs=32M GPS:Sig=4M@-10dBF BW=+-8M@fs=16M		WF:53 BT:69		dB
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – WF mode – BT mode – Power down		2.2 5.8 0.001		mA

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2.6.9.3 Wi -Fi/BT TX

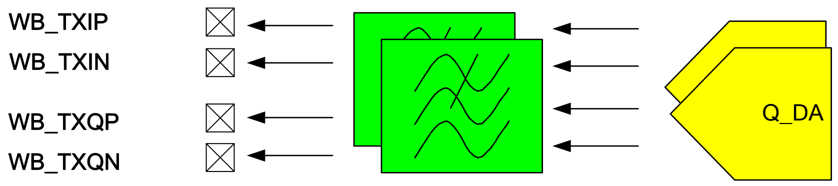

Figure 17. Wi -Fi/BT transmitter analog based-band

2.6.9.4 WB TX Function Specifications

See the table below for the function specifications of the Wi -Fi/BT base-band transmitter.

Table 30. Wi-Fi/BT transmitter specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)		2		V
VCM	Common mode input voltage	0.6	0.65	0.7	V
FS	Input clock frequency Clock rate (WiFi-mode) Clock rate (BT-mode)		480 64		MHz MHz
BW	LPF bandwidth WiFi-mode BT-mode		55 12		MHz
VOS	Differential input referred offset			30	mV
IM3	IM3 WiFi-mode 38M@-11dBm+40M@-11dBm BT-mode 0.5M@4dBm+0.6M@4dBm		WF:60 BT:34		dB
A-die loading			10p//1.3k		F//ohm
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) WF mode BT mode Power down		8.7 3.4 0.001		mA

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2.6.9.5 GPS RX

The GPS receiver (Rx) performs connectivity baseband I/Q channels analog-to-digital conversion:

- Analog input buffer: Deliver driving capability.
- A/D converter: I/Q channels of ADCs perform I/Q digitization for further digital signal processing.

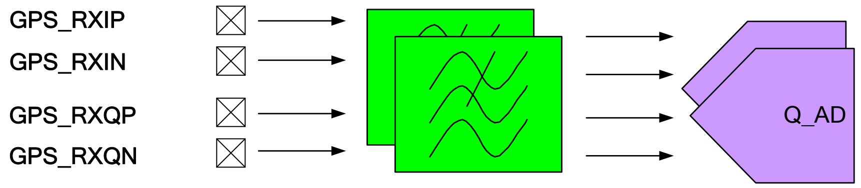

Figure 18. GPS receiver analog based-band

2.6.9.6 GPS Function Specifications

See the table below for the function specifications of the GPS base-band receiver. There are two modes for GPS; one is 16MHz, and the other is 64MHz sampling clock.

Table 31 . GPS receiver specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)		950		mV
VCM	Common mode input voltage	0.5	0.55	0.6	V
FS	Input clock frequency		16 64		MHz
RIN	Differential input resistance	14	20	26	kΩ
VOS	Differential input referred offset			10	mV
DR	Dynamic range GPS:Sig=4M@-10dBF BW=+-8M@fs=16M		52		dB
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel)				

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	– Power on-16MHz mode – Power down		1.8 0.001		mA

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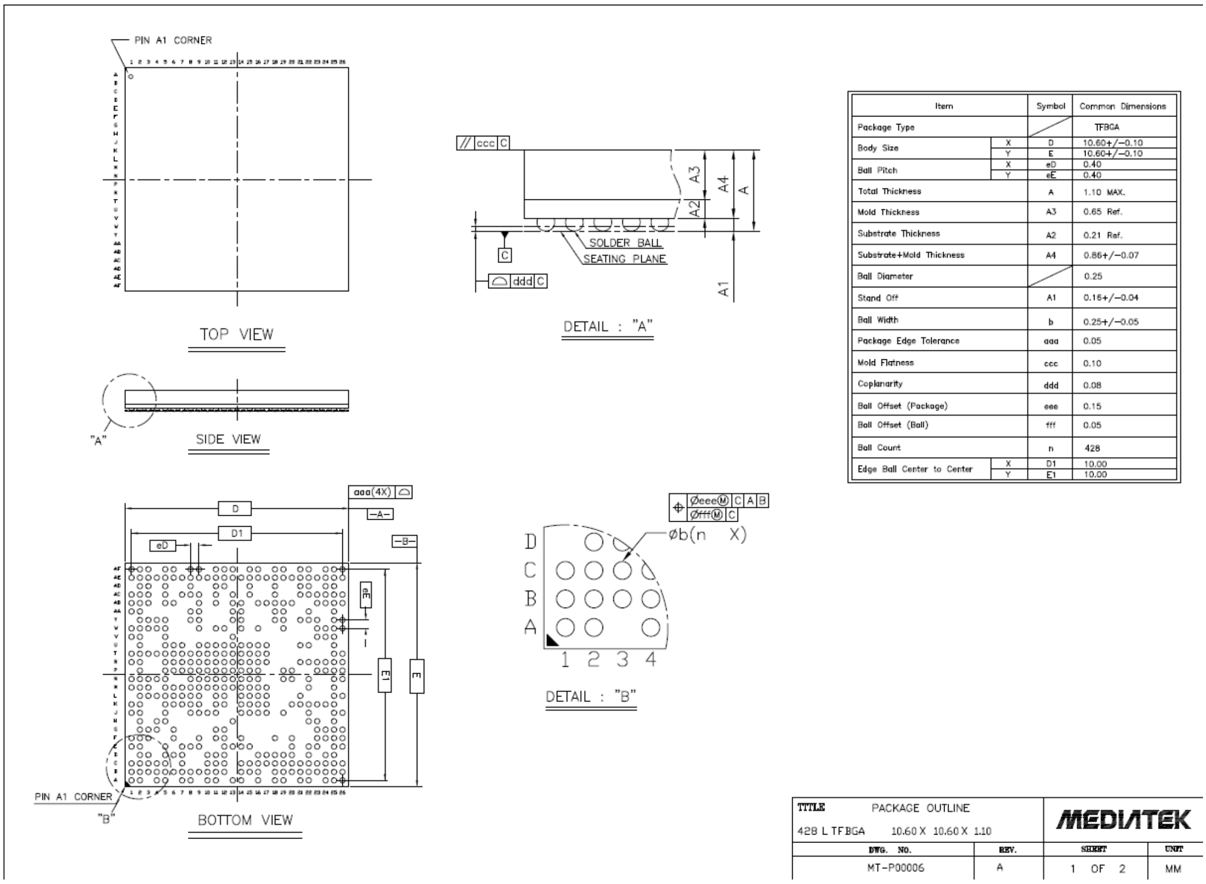
2.7 Package Information

2.7.1 Package Outlines



Item		Symbol	Common Dimensions
Package Type			TFBGA
Body Size	X	D	10.60+/−0.10
	Y	E	10.60+/−0.10
Ball Pitch	X	eD	0.40
	Y	eE	0.40
Total Thickness		A	1.10 MAX.
Mold Thickness		A3	0.65 Ref.
Substrate Thickness		A2	0.21 Ref.
Substrate+Mold Thickness		A4	0.86+/−0.07
Ball Diameter			0.25
Stand Off		A1	0.16+/−0.04
Ball Width		b	0.25+/−0.05
Package Edge Tolerance		aaa	0.05
Mold Flatness		ccc	0.10
Coplanarity		ddd	0.08
Ball Offset (Package)		eee	0.15
Ball Offset (Ball)		fff	0.05
Ball Count		n	428
Edge Ball Center to Center	X	D1	10.00
	Y	E1	10.00

Figure 19 Outlines and dimensions of TFBGA 10.6mm*10.6mm, 428-ball, 0.4mm pitch package

2.7.2 Thermal Operating Specifications

Table 32 Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Maximum operating junction temperature	125	°C	
	Package thermal resistances in nature convection		°C/Watt	

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2.7.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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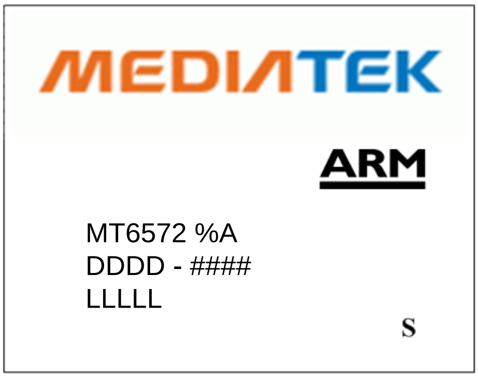
2.8 Ordering Information

2.8.1 Top Marking Definition



MTXXXXXX	Part No.
%:	W : WCDMA T : TD-SCDMA E : Edge
DDDD:	Date Code
####:	Subcontractor Code
LLLLL:	Die Lot No.
S:	Special Code

Figure 20. Top mark of MT6572

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